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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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85775 7590 05/01/2009 Locke Lord Bissell & Liddell LLP Attn: IP Docketing Three World Financial Center New York, NY 10281-2101				
EXAMINER				
FAHERTY, COREY S				
ART UNIT		PAPER NUMBER		
2183				
NOTIFICATION DATE		DELIVERY MODE		
05/01/2009		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ptopatentcommunication@lockelord.com

### Office Action Summary

**Application No.**

10/523,031

**Applicant(s)**

O'SULLIVAN, DANIEL SHANE

**Examiner**

Corey S. Faherty

**Art Unit**

2183

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 April 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 144, 145, 155-158, 160, 164, 165, 167-172 and 1615 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 144, 145, 155-158, 160, 164, 165, 167-172 and 1615 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 03/10/2008
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. This office action is in response to the reply filed on 04/01/2008.
2. Claims 144-145, 155-158, 160, 164-165, 167-172 and 1615 are pending in the application and have been examined.
3. The objection to the drawings made in the previous office action is withdrawn.
4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/01/2008 has been entered.

***Claim Rejections - 35 USC § 112***

5. Claims 144-145, 155-158, 160, 164-165 and 167-172 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. Claim 144 recites the limitation “the elemental processing resource of the first type” in line 8. Because the claim recites two elemental processing resources of the first type, it is unclear which of these two elemental processing resources is being referred to. The scope of the claim is therefore indefinite.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. **Claims 144, 155-156, 164-165 and 167-170** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola (U.S. Patent 5,706,514) in view of Bridges et al. (U.S. Patent 6,081,860), referenced from here forward as Bridges.

10. Regarding claim 144, Bonola discloses a method of execution-instruction delegation between elemental processing resources of at least two different types [abstract], comprising:  
obtaining an execution instruction, wherein the execution instruction is obtained at an elemental processing resource of a first type [col. 3, line 26; a command is encountered by a host, or master, processor];

determining whether an operation-code within the execution instruction should be delegated to an other elemental processing resource [col. 3, lines 25-29; it is determined if the instruction is of a type that cannot be executed by the host processor] of a second type different from the first type [col. 3, lines 36-51; when an encountered instruction is of a type that cannot

currently be executed by the host processor, the host processor transfers data to a slave processor's registers so that the slave processor may execute the instruction];

executing the execution instruction with the processing resource of the first type, if the operation-code within the execution instruction should not be delegated to the other processing resource [col. 3, lines 23-44; if the encountered instruction is not of a type that cannot currently be executed by the host processor, the host processor continues executing it normally]; and

routing the execution instruction to the other elemental processing resource, if the operation-code within the execution instruction is for the other elemental processing resource [col. 3, lines 36-51; when an encountered instruction is of a type that cannot currently be executed by the host processor, the host processor transfers data to a slave processor's registers so that the slave processor may execute the instruction].

Bonola does not explicitly disclose that the system has multiple host, or master, processors each of which delegates instructions to a single slave processor. However, Bonola does teach that other arrangements of multiprocessor computer systems could be used for carrying out the invention [col. 7, lines 11-15]. Bridges discloses such an alternate arrangement for a multiprocessor system having multiple master processors and multiple slave processors [Fig. 1]. Bridges further discloses that multiple master processors issue requests to a slave processor [col. 6, lines 33-36]. Such a system allows for any of the master processors to gain the benefit of having a slave processor. It therefore would have been obvious to a person of ordinary skill in the art at the time the invention was made to have multiple host, or master, processors delegate instruction requests to a slave processor in the system of Bonola because Bridges teaches such a multiprocessor system for handling master processor requests.

11. Regarding claim 155, Bonola in view of Bridges discloses the method of claim 144, wherein the operation-code indicates a type of resource on which to execute [Bonola, col. 3, lines 25-30; an instruction specifies a certain mode of processor on which it can executed].
12. Regarding claim 156, Bonola in view of Bridges discloses the method of claim 144, wherein the other processing resource may be the originating processing resource [Bonola, col. 3, lines 23-44; if the encountered instruction is not of a type that cannot currently be executed by the host processor, the host processor continues executing it normally].
13. Regarding claim 164, Bonola in view of Bridges discloses the method of claim 144, wherein a processing resource is an execution-instruction processing cache [Bonola, col. 3, lines 37-42; the slave processor's registers are used to temporarily hold all data that is necessary for the slave processor to perform the execution provided to it by the host processor].
14. Regarding claim 165, Bonola in view of Bridges discloses the method of claim 144, wherein routing occurs through an execution-instruction signal router [Bonola, col. 3, lines 37-42; the slave processor's registers are used to temporarily hold all data that is necessary for the slave processor to perform the execution provided to it by the host processor; Fig. 1; col. 4, lines 43-45; a host bus is also provided to allow the host processor to communicate with the slave processors].
15. Regarding claims 167, Bonola in view of Bridges discloses the method of claim 144, wherein a processing resource may sleep while another processing resource executes delegated execution-instructions [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; a slave processor may enter a sleep mode while the host processor or other slave processors execute instructions].

16. Regarding claim 168, Bonola in view of Bridges discloses the method of claim 144, wherein the execution-instruction signal causes various processing resources dynamically to turn on and off [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; slave processors may enter a sleep mode in which they do not execute instructions].

17. Regarding claim 169, Bonola in view of Bridges discloses the method of claim 144, wherein the execution-instruction signal from processing resources themselves shuts off processing resources while idling [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; slave processors may enter a sleep mode in which they do not execute instructions].

18. Regarding claim 170, Bonola in view of Bridges discloses the method of claim 144, wherein the execution-instruction signal from processing resources themselves turn on processing resources when execution-instruction signal processing is required [Bonola, col. 8, lines 55-61; col. 9, lines 64-66; a slave processor may be removed from sleep mode when it is necessary for executing instructions that the host processor is unable to execute].

19. **Claims 144-145 and 171-172** are rejected under 35 U.S.C. 103(a) as being unpatentable over Butterworth et al. (U.S. Patent 6,907,454), referenced from here forward as Butterworth, in view of Bridges.

20. Regarding claim 144, Butterworth discloses a method of execution-instruction delegation between elemental processing resources of at least two different types [abstract], comprising:

obtaining an execution instruction, wherein the execution instruction is obtained at an elemental processing resource of a first type [col. 2, lines 48-50; a master processor receives a memory access instruction];

determining whether an operation-code within the execution instruction should be delegated to an other elemental processing resource of a second type different from the first type [col. 2, lines 48-54; the master processor determines that an instruction is of a memory access type and, if it is, determines that it should be sent to a slave processor];

executing the execution instruction with the elemental processing resource of the first type, if the operation-code within the execution instruction should not be delegated to the other elemental processing resource [col. 2, lines 44-58; the master processor executes non-memory access instructions normally];

routing the execution instruction to the other elemental processing resource, if the operation-code within the execution instruction is for the other elemental processing resource [col. 2, lines 53-54; for memory access instructions, the master processor writes a request to the slave processor to carry out the instruction].

Butterworth does not explicitly disclose that the system has multiple master processors each of which delegates instructions to a single slave processor. Bridges discloses a multiprocessor system having multiple master processors and multiple slave processors [Fig. 1]. Bridges further discloses that multiple master processors issue requests to a slave processor [col. 6, lines 33-36]. Such a system allows for any of the master processors to gain the benefit of having a slave processor. It therefore would have been obvious to a person of ordinary skill in the art at the time the invention was made to have multiple master processors delegate instruction requests to a slave processor in the system of Butterworth because Bridges teaches such a multiprocessor system for handling master processor requests.



21. Regarding claim 145, Butterworth in view of Bridges discloses the method of claim 145, but does not explicitly disclose that the method is completed within a single processing cycle.

The purpose of the Butterworth design is to reduce the processing delay of a memory operation [col. 1, lines 59-65]. Instead of forcing a processor to incur all of the delay necessary for executing a memory operation, the processor instead delegates the operation to a second processor [col. 2, lines 44-58]. If the first processor is able to perform this delegation quickly, it can continue executing other instructions [col. 5, lines 50-51] while the second processor performs the memory operation. The fewer clock cycles it takes for the first processor to perform the delegation, the more time the first processor will have to execute other instructions while the second processor is performing the memory operation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to complete the instruction-delegation method disclosed in Butterworth in a single processing cycle because doing so would allow the master processor to begin executing other instructions more quickly and thus execute more code overall while the slave processor is performing a memory operation.

22. Regarding claim 171, Butterworth in view of Bridges discloses the method of claim 144, wherein processing resources are communicatively disposed on a same die [Butterworth, col. 4, lines 36-40; a bridge device for communication between the memory and the slave processor may be integrated into a single chip package with the slave processor].

23. Regarding claim 172, Butterworth in view of Bridges discloses the method of claim 171, wherein an execution-instruction signal router is on the same die with processing resources

[Butterworth, col. 4, lines 36-40; a bridge device for communication between the memory and the slave processor may be integrated into a single chip package with the slave processor].

24. **Claims 157-158, 160 and 1615** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola in view of Bridges as applied to claim 144 above, and further in view of Mohamed et al. (U.S. Patent 5,978,838), referenced from here forward as Mohamed.

25. Regarding claims 157, 160 and 1615, Bonola in view of Bridges does not explicitly disclose that the first type of processing resource is an integer-processing unit nor that the other type of processing resource is a vector processing resource.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 61-67]. The system includes integer-processing units for executing integer instructions [col. 5, lines 8-15]. The system also includes a vector processor [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an integer-processing unit as a processing resource in the system of Bonola because Mohamed discloses doing including an integer-processing unit in a multi-processor system [col. 5, lines 8-15] and doing so allows the system to execute integer instructions. Furthermore, without an integer-processing unit, the system of Bonola would be unable to execute integer instructions, greatly limiting the amount of software that it could run.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a vector-processing unit as a processing resource in the system of Bonola because Mohamed discloses including a vector processor in a multi-processor system [abstract] and doing so allows a system to more efficiently execute vector instructions without impacting

the execution efficiency of a main processor. The addition of a vector processing mode to a slave processor in the system of Bonola would allow the host processor to delegate vector operations to slave processors while continuing to execute other instructions, resulting in greater processing efficiency.

26. Regarding claim 158, Bonola in view of Bridges does not explicitly disclose that a processing resource is a mathematical processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 19-26]. The system includes a math co-processor [col. 1, line 24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mathematical processing unit as a processing resource in the system of Bonola because Mohamed discloses including a math processor in a multi-processor system [col. 1, lines 19-26] and doing so allows the system to more efficiently execute mathematical operations. The use of a mathematical processor as a slave processor in the system of Bonola allows the host processor to be designed for better execution of other types of instructions, allowing for greater overall processing efficiency. Furthermore, the addition of a mode in which a slave processor behaves a mathematical processor allows the system of Bonola to execute mathematical operations, also potentially increasing overall processing efficiency.

***Response to Arguments***

27. Applicant has not submitted any new arguments. The positions of the office remain as stated in the previous office action.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/  
Supervisory Patent Examiner, Art Unit 2183

/Corey S Faherty/  
Examiner, Art Unit 2183